IN THE SPECIFICATION:

Please replace paragraph number **[0030]** with the following rewritten paragraph:

[0030] For example, vision systems, such as PRS, can be used to examine structural defects such as broken leads, dendrite growth, solder resist irregularities, oxide contamination, corrosion, etc. In this step, the vision system will typically compare pictures of lead frame fingers, bond pads, and other features on and around the individual semiconductor die ~~sites 60~~ sites to a predetermined known good template. Electrical testing can also be accomplished, for example, by using various automated or other test equipment, including curve tracer testing, test probes, RF testing, and the like. Tests screening for intermittent failures, such as high temperature reverse-bias (HTRB) tests, vibration testing, temperature cycling, and mechanical shock testing, etc. are also contemplated by the present invention, as well as tests for solderability, microcorrosion, noise characterization, electromigration stress, electrostatic discharge, plating defects, etc. The results of the different tests are fed into a computer, compiled, and correlated with individual semiconductor die ~~sites 60~~ sites on a particular mounting substrate ~~array 10.~~ array.

Please replace paragraph number **[0034]** with the following rewritten paragraph:

[0034] Illustrated in drawing FIG. 4 is a semicompleted BGA chip package which includes an aperture 54 having bond pads 56 located along opposing sides of the aperture 54. Bond pads 56 are selectively provided with an electrically conductive trace 58 that leads to a respective conductive element, solder ball or solder ball location 160. Selected conductive elements, or solder balls ~~60, are~~ 160, are provided with a second circuit trace 62 leading to a respective test contact pad 64 located outwardly away from aperture 54 and solder ~~balls 60.~~ balls 160. Test contact pads 64 are preferably arranged to fan-out in what is referred to as thin small outline package (TSOP), which is recognized as an industry standard.

Please replace paragraph number **[0035]** with the following rewritten paragraph:

[0035] As can be seen in drawing FIG. 4, individual chip circuitry portion 70 includes various circuit traces 58 and 62 which interconnect bond pads 56 to solder balls ~~60 and~~ 160 and which further interconnect solder balls ~~60 to~~ 160 to peripherally located test contact pads 64 and are able to be easily routed around any solder balls ~~60 in~~ 160 in a somewhat serpentine fashion to circumvent one or more particular solder balls that would otherwise physically block the circuit from reaching its respective destination. This particular characteristic of being able to route circuit traces as needed around intervening solder balls ~~60, or~~ 160, or alternative connective elements used in connection with, or in lieu of solder balls, allows great versatility in that solder ball grid arrays having virtually any feasible number of solder balls arranged in any feasible pattern could be used and need not be restricted to the exemplary column arrangement as shown in drawing FIG. 4. It should be appreciated that although substrate tape outline 50 provides a convenient, cost efficient method of providing the desired circuit traces and ball grid array on a selected substrate, alternative methods to apply circuit traces to a substrate can be used. For example, circuit layers including circuit traces, bond pads, solder balls, or contact elements, and/or test contact pads could be screen printed onto one or both faces of a substrate. Furthermore, multiple layers of circuit layers can be disposed upon not only the exposed surfaces of the supporting substrate, but circuit layers could be "sandwiched" or laminated within the substrate by circuit layer lamination methods known in the art if so desired. Resist can be placed on any of these features and can be removed via a process with the use of a laser.

Please replace paragraph number **[0036]** with the following rewritten paragraph:

[0036] Described in drawing FIG. 5 is a board-on-chip assembly ~~110.~~ 1110. A packaged, flip-chip type semiconductor device incorporating teachings of the present invention, as shown in drawing FIG. 5, has conductive structures protruding therefrom in a ball grid array pattern and includes a semiconductor die 20 and a substrate, which is also referred to herein as an interposer 30. The interposer 30 may be roughened by a laser to increase the surface area for better attachment to the semiconductor die 20.